UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,832	06/27/2003	Young Mau Kim	049128-5106	4827

9629 7590 01/23/2006

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER
SHERMAN, STEPHEN G

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,832	KIM ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16 and 18-24* is/are rejected.

7)☐ Claim(s) *8 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 6 December 2005.

Claims 1-24 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-7 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Payne (US 5,429,779) in view of Ito et al. (US 2002/0021097).

Regarding claim 1, Payne discloses an inverter device (Figure 1, item 11) for a liquid crystal display, comprising:

a transformer (Figure 2C, item T1) for receiving an inverter drive voltage, converting the received drive voltage into an AC lamp drive voltage and supplying the AC lamp drive voltage to a high path of a backlight lamp (Column 5, lines 7-14); and

a low path switching part (Figures 2A-2D, items Q2 and QX1 are connected to the low path of the backlight lamp CCFL through connection 108.); and

a shutdown circuit (Figure 1, item 15) for receiving a voltage input (Figure 1, item 106) through the low path of the backlight lamp (Figure 1, item 108) to monitor for a malfunction of the backlight lamp in response to an external shutdown ON/OFF signal (Column 3, lines 33-37.The examiner interprets the signal sent to disable the inverter circuit to be the shutdown ON/OFF signal).

Payne fails to teach of an inverter device for a liquid crystal display comprising a low path switching part selectively connecting a low path of the backlight lamp with a ground voltage source in response to an external inverter ON/OFF signal.

Ito et al. discloses a lighting circuit for an electronic discharge lamp comprising a low path switching part selectively connecting a low path of a lamp with a ground voltage source in response to an external inverter ON/OFF signal (Figure 4, sw4 and paragraph [0048]. The examiner interprets that the signal which is given from a drive circuit is a external ON/OFF signal since the signal would turn switch sw4 on or of which would selectively connect the lamp to the ground source.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the low path switching part configuration taught by Ito et al. with the inverter device taught by Payne in order to enhance safety by reducing the difference in electric potential of the voltage supply line with respect to the ground electric potential.

Regarding claim 2, Payne and Ito et al. disclose the device according to claim 1.

Payne also discloses wherein the low path switching part includes:

a first driver (Figures 2A, 2B, 2C and 2D, items Q5 and Q6) selectively supplying the inverter drive voltage to the low path of the backlight lamp in response to the inverter ON/OFF signal (Figures 2A, 2B, 2C and 2D, items Q5 and Q6 can supply a voltage to the low path of the backlight lamp in response to the ON/OFF signal, ENABLE. Q5 receives the ON/OFF signal through U1 connection 1, then the driver, Q5 and Q6, supplies the inverter drive voltage, VCC, which is also received through U1 connection 1, to the first switching part which is connected to the low path of the backlight lamp); and

a first switching part (Figures 2A, 2B, 2C and 2D, items QX1 and Q2) connecting the low path of the backlight lamp to the ground voltage source in response to an output signal of the first driver (Figures 2A, 2B, 2C and 2D, items QX1 and Q2 are connected to the low path of the backlight lamp through the connection between Q2 and Q14, Q14 being connected to item 108, the low path of the lamp. Q2 is then connected to QX1, which is connected to ground. Q2 receives an output signal from Q6 and Q5, the driver,

which would therefore allow Q2 and QX1 to connect 108, the low path of the backlight lamp, to ground).

Regarding claim 3, Payne and Ito et al. disclose the device according to claim 2. Payne also discloses the first driver (Figures 2A, 2B, 2C and 2D, items Q5 and Q6) includes:

a first switch being switched in response to the inverter ON/OFF signal (Figures 2A, 2B, 2C and 2D, item Q5 is switched in response to ENABLE, the inverter ON/OFF signal, through U1 connection 1); and

a second switch supplying the inverter drive voltage to the first switching part in response to a state of the first switch (Figures 2A, 2B, 2C and 2D, item Q6 can supply the inverter drive voltage, VCC, which it receives through U1 connection 1, to the first switching part, Q2 and Qx1).

Regarding claim 4, Payne and Ito et al. disclose the device according to claim 3. Payne also discloses wherein the first switching part (Figures 2A, 2B, 2C and 2D, items Q2 and QX1) includes:

first and second field effect transistors (Q2 and Qx1 are shown in Figure 2A to be FETs) connected in series between the low path of the backlight lamp and the ground voltage source for connecting the low path of the backlight lamp to the ground voltage source in response to an output signal of the second switch (Figures 2A, 2B, 2C and 2D, items QX1 and Q2 are connected to the low path of the backlight lamp through the

connection between Q2 and Q14, Q14 being connected to item 108, the low path of the lamp. Q2 is then connected to QX1, which is connected to ground. Q2 receives an output signal from Q6, the second switch, which would therefore allow Q2 and QX1 to connect 108, the low path of the backlight lamp, to ground); and

a resistor (Figure 2D, item R3) connected between the low path of the backlight lamp and the first field effect transistor (Figures 2A, 2B, 2C and 2D, item R3 is connected to 108, the low path of the backlight lamp, and also connected to the first field effect transistor, Q2, through the connection between Q2 and Q14 and then through line 106).

Regarding claim 5, Payne and Ito et al. disclose the device according to claim 1.

Payne also discloses wherein the shutdown circuit includes:

a second driver (Figures 2A, 2B, 2C and 2D, items Q6 and Q5) selectively supplying the inverter drive voltage to the low path of the backlight lamp in response to the-shutdown ON/OFF signal (Figures 2A, 2B, 2C and 2D, items Q5 and Q6 supply the inverter drive voltage VCC through U1 connection 1 to the low path of the backlight lamp through Q2 in response to ENABLE which is received through U1 connection 1);

a second switching part (Figures 2A, 2B, 2C and 2D, items Q13 and Q14) providing one of an enabling and disabling shutdown function for monitoring for the presence or absence of a malfunction of the backlight lamp in response to an output signal of the second driver (Figures 2A, 2B, 2C and 2D, items Q13 and Q14 are a part of item 15 of Figure 1. Column 3, lines 33-37 states that a detection circuit sends a

signal to disable the inverter circuit if a malfunction is detected. The examiner interprets this as providing either an enabling or disabling function, and as seen in Figures 2A, 2B, 2C and 2D, Q13 can receive a signal from Q6 of the second driver through its connection to Q2); and

an error amplifier monitoring for the presence or absence of a malfunction of the backlight lamp when the shutdown function is enabled by the second switching part (Figure 1, items 15 and 106 and column 5, lines 24-25. The examiner interprets this to mean that monitoring is occurring at all times which would also be when the shutdown function is enabled by the second switching part).

Regarding claim 6, Payne and Ito et al. disclose the device according to claim 5.

Payne also discloses wherein the second driver (Figures 2A, 2B, 2C and 2D, items Q5 and Q6) includes:

a third switch being switched in response to the shutdown ON/OFF signal (Figures 2A, 2B, 2C and 2D, item Q5 is switched in response to ENABLE, the inverter ON/OFF signal, through U1 connection 1); and

a fourth switch supplying the inverter drive voltage to the second switching part in response to a state of the third switch (Figures 2A, 2B, 2C and 2D, item Q6 can supply the inverter drive voltage, VCC, which it receives through U1 connection 1, to the second switching part, Q13 and Q14).

Regarding claim 7, Payne and Ito et al. disclose the device according to claim 6.

Payne also discloses wherein the second switching part (Figures 2A, 2B, 2C and 2D, items Q13 and Q14) includes:

third and fourth field effect transistors (Figures 2A, 2B, 2C and 2D, items Q13 and Q14 are FETs) connected in series between the low path of the backlight lamp and the ground voltage source for connecting the low path of the backlight lamp to the ground voltage source in response to an output signal of the fourth switch (Figures 2A, 2B, 2C and 2D, items Q13 and Q14 are connected to the low path of the backlight lamp through Q14 which is connected to item 108, the low path of the lamp. Q14 is connected to ground through C9. Q13 receives an output signal from Q6, the second switch, through Q2 which would therefore allow Q13 and Q14 to connect 108, the low path of the backlight lamp, to ground); and

a resistor (Figure 2D, item R3) connected between the low path of the backlight tamp and the third field effect transistor (Figures 2A, 2B, 2C and 2D, item R3 is connected to 108, the low path of the backlight lamp, and also connected to the first field effect transistor, Q14 through line 106).

Regarding claim 18, this claim is rejected under the same rationale as claim 1.

Regarding claim 19, this claim is rejected under the same rationale as claim 2.

Regarding claim 20, this claim is rejected under the same rationale as claim 3.

Regarding claim 21, this claim is rejected under the same rationale as claim 4.

Regarding claim 22, this claim is rejected under the same rationale as claim 5.

Regarding claim 23, this claim is rejected under the same rationale as claim 6.

Regarding claim 24, this claim is rejected under the same rationale as claim 7.

5. Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Payne (US 5,420,779) in view of Ito et al. (US 2002/0021097) and further in view of Lin et al. (US 2003/0001524).

Regarding claim 9, Payne discloses a backlight lamp monitoring device for a liquid crystal display, comprising:

a backlight lamp (Figure 1, CCFL); and

an inverter (figure 1, item 11) receiving an inverter drive voltage, converting the received drive voltage into an AC lamp drive voltage, and supplying the AC lamp drive voltage to a high path of the backlight lamp (Column 5, lines 7-14);

wherein the inverter selectively connects a low path of the backlight lamp with a ground voltage source in response to an external inverter ON/OFF signal (Figures 2A, 2B, 2C and 2D, items Q2 and QX1 are connected to the low path of the backlight lamp

CCFL through connection 108 and also connected to ground. Items Q2 and QX1 can be switched by the ON/OFF signal, ENABLE); and

the inverter receives a voltage input through the low path of the backlight lamp to perform a shutdown function for monitoring for the presence or absence of a malfunction of the backlight lamp in response to an external shutdown ON/OFF signal (Figure 1, item 15 receives a voltage input through line 106 from the backlight lamp connection 108. In column 3, lines 33-37 the examiner interprets the signal sent to disable the inverter circuit to be the shutdown ON/OFF signal).

Payne fails to teach of a backlight lamp monitoring device for a liquid crystal display wherein the inverter selectively connects a low path of the backlight lamp with a ground voltage source in response to an external inverter ON/OFF signal.

Ito et al. discloses a lighting circuit for an electronic discharge lamp comprising a low path switching part selectively connecting a low path of a lamp with a ground voltage source in response to an external inverter ON/OFF signal (Figure 4, sw4 and paragraph [0048]. The examiner interprets that the signal which is given from a drive circuit is a external ON/OFF signal since the signal would turn switch sw4 on or of which would selectively connect the lamp to the ground source.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the low path switching part configuration taught by Ito et al. with the inverter device taught by Payne in order to enhance safety by reducing the difference in electric potential of the voltage supply line with respect to the ground electric potential.

Payne and Ito et al. fail to teach of a backlight lamp monitoring device for a liquid crystal display, comprising: a plurality of backlight lamps; and a plurality of inverters, each receiving an inverter drive voltage.

Lin et al. discloses a plurality of backlight lamps (Figure 2, Lp1 and Lp2); and a plurality of inverters (Figure 2, items 10 and 20), each receiving an inverter drive voltage (Figure 2, items 10 and 20 both receive and input Vin).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Payne, Ito et al. and Lin et al. in order to provide a plurality of lamps and inverters in a device.

Regarding claim 10, this claim is rejected under the same rationale as claim 1.

Regarding claim 11, this claim is rejected under the same rationale as claim 2.

Regarding claim 12, this claim is rejected under the same rationale as claim 3.

Regarding claim 13, this claim is rejected under the same rationale as claim 4.

Regarding claim 14, this claim is rejected under the same rationale as claim 5.

Regarding claim 15, this claim is rejected under the same rationale as claim 6.

Regarding claim 16, this claim is rejected under the same rationale as claim 7.

Allowable Subject Matter

6. Claims 8 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: The primary reason for allowance of the claims is the inclusion of the limitation of including a capacitor connected between a drain terminal of the third field effect transistor and a drain terminal of the fourth field effect transistor and also a capacitor connected between the drain terminal of the fourth field effect transistor and the ground voltage source for an inverter device of a liquid crystal display, of which could not be found in the prior art.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miyoshi (US 2002/0109465) discloses of connecting a control switch between a lamp and aground path.

Bergeson et al. (US 4,064,414) discloses of connecting a control switch between a lamp and a ground path.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER